

CS 315-01 Lab RISC-V Machine Code

Lab 03 Tue Oct 3

Project 04 Tue Oct 10

IG Wed Oct 11

Midterm Thu Oct 12

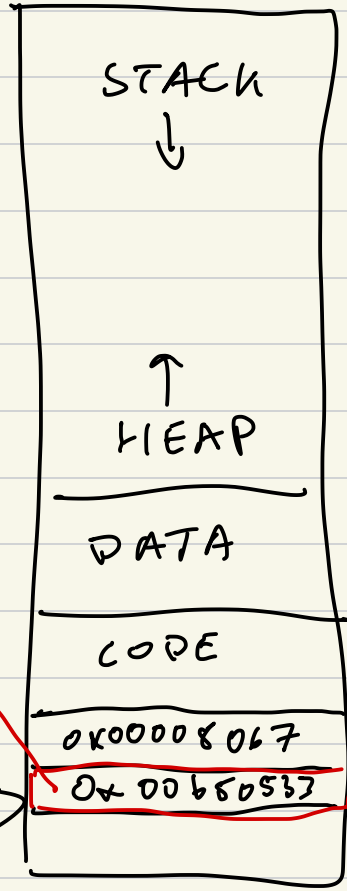
Machine Code \leftarrow Binary form
of Assembly

RISC-V Emulator lab 03 \rightarrow Project 04

Dynamic analysis project 07

Cache Simulation project 09

Memory



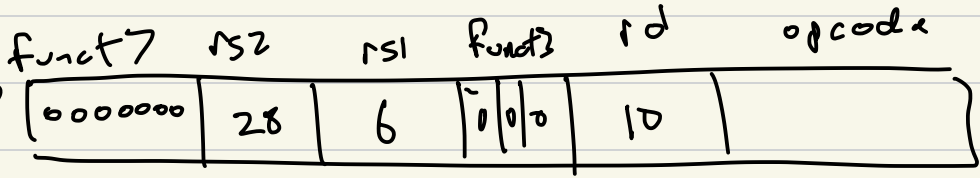
```
uint32_t iw;  
uint32_t *pc;
```

PC ← iw = *pc

addr ->

```
uint64_t regs[32];
```

add a0, t1, t3



0x 0 0 B 5 0 5 3 3

0000 0000 1011 0101 0000 0101 0011 0011
Mnemonic Δ
0000 0000 0111 1111